CLAIMS

1. A stack of semiconductor packages comprising:

first and second semiconductor packages,

wherein each of the first and second semiconductor packages comprises an insulative substrate including a central opening extending through the substrate from a first surface to an opposite second surface of the substrate, circuit patterns on the first and second surfaces, vias through the substrate electrically coupling at least some of the circuit patterns of the first and second surfaces, stacked first and second semiconductor chips within the opening without contacting the substrate, with each said semiconductor chip having an active surface with bond pads thereon and an opposite inactive surface, bond wires electrically coupling the bond pads of the semiconductor chips to the circuit patterns, conductive balls fused to the circuit patterns of the second surface of the substrate, and an encapsulant within the opening and covering the first and second semiconductor chips and at least one of the first and second surfaces of the substrate without covering the inactive surface of one of the first and second semiconductor chips, and

wherein the first semiconductor package is stacked on the second semiconductor package so that the conductive balls of the first semiconductor chip face and are fused to the circuit patterns of the first surface of the substrate of the second semiconductor package.

2. The stack of claim 1, wherein the active surfaces and bond pads of the first and second semiconductor chips of the first and second semiconductor packages are oriented in a same direction.

3. The stack of claim 2, wherein the first semiconductor chip has a smaller perimeter than the second semiconductor chip.

4. The stack of claim 2, wherein a perimeter of the first and second semiconductor chips is a same size, but the bond pads of the first or second semiconductor chip having the exposed inactive surface are not superimposed by the other of the first or second semiconductor chips.

5. The stack of claim 2, wherein the first and second semiconductor chips are a same size.

6. The stack of claim 2, wherein the active surfaces and bond pads of the first and second semiconductor chips are oriented toward the first surface of the substrate.

7. The stack of claim 2, wherein the active surfaces and bond pads of the first and second semiconductor chips are oriented toward the second surface of the substrate.

8. A stack of semiconductor packages comprising:

first and second semiconductor packages,

wherein each of the first and second semiconductor packages comprises an insulative substrate including a central opening extending through the substrate from a first surface to an opposite second surface of the substrate, circuit patterns on the first and second surfaces, vias through the substrate electrically coupling at least some of the circuit patterns of the first and second surfaces, stacked first and second semiconductor chips within the opening without contacting the substrate, with each said semiconductor chip having an active surface with bond pads thereon and an opposite inactive surface, the active surfaces being oriented toward the first surface of the substrate, bond wires electrically coupling the bond pads of the semiconductor chips to the circuit patterns, conductive balls fused to the circuit patterns of the second surface of the substrate, and an encapsulant within the opening and covering the first and second semiconductor chips and the first surface of the substrate, the second surface of the substrate and the inactive surface of the second semiconductor chip being in a common horizontal plane and uncovered by the encapsulant, and

wherein the first semiconductor package is stacked on the second semiconductor package so that the conductive balls of the first semiconductor chip face and are fused to the circuit patterns of the first surface of the substrate of the second semiconductor package.

9. The stack of claim 8, wherein the first semiconductor chip has a perimeter smaller than a perimeter of the second semiconductor chip.

10. The stack of claim 9, wherein the first and second semiconductor chips have a same size perimeter.

11. The stack of claim 10, wherein the bond pads of the second chip are not superimposed by the first chip.

12. The semiconductor chip of claim 10, wherein the first and second semiconductor chips have bond pads only along two opposite edges of the active surface, and the bond pads of the second semiconductor chip are not superimposed by the first semiconductor chip.

13. A stack of semiconductor packages comprising:

first and second semiconductor packages,

wherein each of the first and second semiconductor packages comprises an insulative substrate including a central opening extending through the substrate from a first surface to an opposite second surface of the substrate, circuit patterns on the first and second surfaces, vias through the substrate electrically coupling at least some of the circuit patterns of the first and second surfaces, stacked first and second semiconductor chips within the opening without contacting the substrate, with each said semiconductor chip having an active surface with bond pads thereon and an opposite inactive surface, the active surfaces being oriented in a same direction, bond wires electrically coupling the bond pads of the semiconductor chips to the circuit patterns, conductive balls fused to the circuit patterns of the second surface of the substrate, and an encapsulant within the opening and covering the first and second semiconductor chips and the one of the first or second surfaces of the substrate without covering the other of the first or second surfaces of the substrate and the inactive surface of at least one of the first and second semiconductor chips, wherein the first semiconductor package is stacked on the second semiconductor package so that the conductive balls of the first semiconductor chip face and are fused to the circuit patterns of the first surface of the substrate of the second semiconductor package.

14. The stack of claim 13, wherein the first semiconductor chip has a perimeter smaller than a perimeter of the second semiconductor chip.

15. The stack of claim 13, wherein the first and second semiconductor chips have a same size perimeter.

16. The stack of claim 15, wherein the bond pads of the second chip are not superimposed by the first chip.

17. The stack of claim 16, wherein the first and second semiconductor chips have bond pads only along two opposite edges of the active surface, and the bond pads of the second semiconductor chip are not superimposed by the first semiconductor chip.

18. The stack of claim 13, wherein the bond pads of the first and second semiconductor chips are oriented toward the first surface of the substrate.

19. The stack of claim 13, wherein the bond pads of the first and second semiconductor chips are oriented toward the second surface of the substrate.

20. The stack of claim 13, wherein the second surface of the substrate is uncovered by the encapsulant.